5. (Original) A method comprising:

preparing a substrate;

forming a first gate structure including a PWELL without using a mask; and

forming a second gate structure including an NWELL using only one mask.

6. (Original) The method of claim 5, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL.

7. - 8. (Previously Withdrawn)

9. (Original) A method comprising:

preparing a substrate;

forming a first gate structure including a PWELL having a depth of about 200 nanometers without using a mask; and

forming a second gate structure including an NWELL using only one mask.

10. (Original) The method of claim 9, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL.

11. - 16. (Previously Withdrawn)

17. (Original) A method comprising:

preparing a substrate;

forming a first gate structure including only blanket implants; and

forming a second gate structure including an NWELL using only one mask.

18. (Original) The method of claim 17, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming an NWELL having a depth of about 200 nanometers.

19. - 35. (Previously Withdrawn)

36. (Currently Amended) A method of forming one or more dual gate structures, the method comprising:

forming one or more gate structures including a PWELL without a mask;

masking one or more [NWELL] PWELL regions; and

forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

38. (Amended) A method of forming one or more dual gate structures, the method comprising:

forming one or more gate structures including a PWELL using blanket implants;

masking one or more [NWELL] PWELL regions; and

forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

45. (Previously Added) The method of claim 1, preparing the substrate comprises forming a PWELL in an *n*-type substrate.

46. (Previously Added) The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises forming one or more complementary metal-oxide semiconductor dual gate structures in the substrate using only one mask.

47. (Previously Added) The method of claim 2, wherein forming the sacrificial oxide layer on the semiconductor comprises growing a sacrificial oxide layer to a depth of a few microns.

48. (Previously Added) The method of claim 3, wherein forming the gate oxide layer on the semiconductor comprises forming the gate oxide layer having a thickness of between about five nanometers and about ten nanometers.

49. (Previously Added) The method of claim 5, wherein preparing the substrate comprises forming a PWELL in an *n*-type substrate.

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50. (Previously Added) The method of claim 5, wherein forming the first gate structure including the PWELL without using the mask comprises forming the PWELL by a blanket implant of boron ions at about 430 keV.

51. (Previously Added) The method of claim 5, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a depth of about 200 nanometers.

52. (Previously Added) The method of claim 5, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a blanket implant of boron ions at about 430 keV and a depth of about 200 nanometers.

53. (Previously Added) The method of claim 49, wherein forming the first gate structure including the PWELL without using the mask comprises forming the PWELL by a blanket implant of boron ions at about 430 keV.

54. (Previously Added) The method of claim 49, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a depth of about 200 nanometers.

55. (Previously Added) The method of claim 9, wherein preparing the substrate comprises forming a PWELL in an *n*-type substrate.